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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,606	02/19/2004	Jae-Hee Oh	9862-000026/US	3174

30593 7590 06/14/2007
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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,606	OH ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-22* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 10-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. (6,503,794).

Regarding claim 1, Watanabe et al. teach in figure 1 and related text a semiconductor device comprising:

a cell array region A formed in a semiconductor substrate and including a capacitor having a lower electrode 25, 27 and an upper electrode 29, the lower electrode having a lower electrode height;

a peripheral circuit region B formed in the semiconductor substrate and including a first metal wiring, the first metal wiring 31 having a first metal height, and having a lower surface in a substantially planar orientation with a lower surface of the lower electrode 16 (the lower surface is touching the semiconductor substrate);

a first insulating layer 18 formed on the cell array region and the peripheral circuit region and having openings; and

a second insulating layer 23, 28, 33, 37 formed on the first insulating layer 18, the first metal wiring 31 being arranged in the second insulating layer,

wherein the second insulating layer includes a first sub-layer 23 surrounding the first metal wiring 31 and a second sub-layer 28, 33, 37 formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer 33 that is formed substantially along the entire substrate and between the upper electrode 29 and the first metal wiring 31, and an entire upper layer 37 that is formed substantially along the entire substrate and over the upper electrode 29,

and the first sub-layer is distinct from the second sub-layer.

Regarding claims 2 and 5-8, Watanabe et al. teach in figure 1 and related text a first conductive plug (part of 25) extending through the first insulating layer to connect the lower electrode to the semiconductor substrate; and

a second conductive plug (part of 31) extending through the first insulating layer to connect the first metal wiring to the semiconductor substrate.

first gate structures (including source and drain) formed in the cell array region, the first insulating layer being formed on the first gate structures;

second gate structures (including source and drain) formed in the peripheral region, the first insulating layer being formed on the second gate structures;

a first storage node contact hole and a first bit line contact hole 12, 28 formed through the first insulating layer for exposing a first surface of the substrate in the cell array region;

first metal contact holes formed through the first insulating layer for exposing the first and second gate structures and a second surface of the substrate in the peripheral region;

conductive plugs formed in the first storage node contact hole, the first bit line contact hole and the first metal contact hole, the first metal wiring being in electrical contact with the conductive plug in the first metal contact hole;

a capacitor formed in the second insulating layer in the cell array region, the capacitor being in electrical contact with the conductive plug in the first storage node contact hole; and

a second metal wiring 35 formed on the second insulating layer in the peripheral region, the second metal wiring being electrically connected to the first metal wiring,

wherein the peripheral region includes at least one of core circuitry peripheral circuitry and logic circuitry,

wherein the capacitor has a metal/insulator/metal structure, and

a bit line formed on the second insulating layer and electrically connected to the conductive plug in the first bit line contact hole through a second bit line contact hole formed through the second insulating layer, wherein the bit line and the second metal wiring are formed from a single metal layer.

Response to Arguments

Applicant argues that Watanabe et al. do not teach in figure 1 and related text a lower layer that is formed substantially along the entire substrate and between the upper electrode and the first metal wiring, and an entire upper layer that is formed substantially along the entire substrate and over the upper electrode.

The lower layer 33 of Watanabe et al. is formed substantially along the entire substrate and between the upper electrode 29 and the first metal wiring 31, wherein the entire upper layer 37 is formed substantially along the entire substrate and over the upper electrode 29. Therefore, Watanabe et al. teach in figure 1 and related text a lower layer that is formed substantially along the entire substrate and between the upper electrode and the first metal wiring, and an entire upper layer that is formed substantially along the entire substrate and over the upper electrode, as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/11/07

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800